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# Construction and Operation of Three-Dimensional Memory and Logic Molecular Devices and Circuits

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**14. ABSTRACT**

We set out to show proof-of-concept of fabricating molecular transistors which could be used as the basis for future molecular circuits. During the research, we demonstrated two new types of metal-oxide semiconductor transistors: vertical metal-insulator tunneling transistors (MITTs) and an additional device in which a self-assembled fullerene monolayer is coupled to a MITT. The presence of the molecular layer allows the transistor to exhibit higher currents and less leakage.

We also constructed a ferrocene-based self-assembling monolayer attached to gold nanoparticles, exhibiting a gate effect which allows control of the transistor rectification via the gate voltage. The theoretical model to support this, and the fabrication and control techniques used to produce the device, may provide new insights on gated molecular junctions.

Finally, we explored three-dimensional logic and memory devices in the form of resonant tunnel diodes (RTDs) used in the pre-CMOS era to construct digital circuits but with prohibitive fabrication costs. We demonstrated a low-cost plastic-based NDR device with highly-reproducible electronic characteristics, and constructed a simple digital circuit from them demonstrating two NDR devices in series acting as an "AND" logic gate.

**15. SUBJECT TERMS**

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**Construction and operation of three dimensional memory and logic molecular devices and circuits**

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# 1 General

During the last four years we focused on the development of novel molecular devices and circuits. The goal was to show the proof-of concept of fabrication a set of reliable molecular transistors in a parallel fashion which, in turn can be used as basis for future molecular circuits. This report summarizes our results.

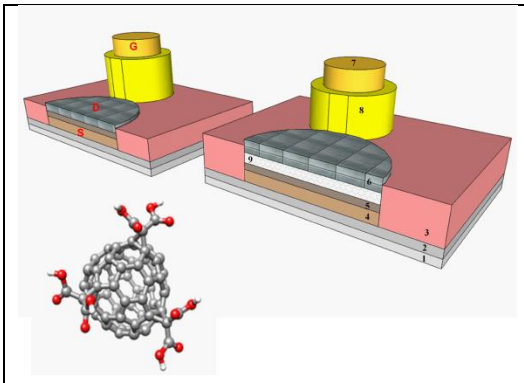
I would like to thank the US-Airforce fund and especially to Dr. Harold Weinstock for the support.

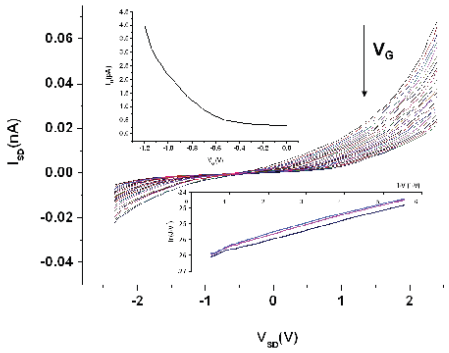
# 2 Summary of Main Results

## 2.1 Post-Complementary Metal Oxide Semiconductor vertical and molecular transistors; a platform for molecular electronics

During the research term we have demonstrated two new types of post complementary metal-oxide semiconductor transistors- vertical metal- insulator tunneling transistor (MITT) and additional device in which a self-assembled monolayer is coupled to it (M-

MITT figure 1). For the molecular layer, we choose a fullerene derivatives (Figure 1). These $C_{60}$-based compounds have shown promising properties such as single-electron charging and switching, which makes them important candidates for future memory and logic applications. In our study, a modified Self-Assembled Monolayer (SAM) composed of $C_{60}$ derivative, carboxyfullerene (CF) was utilized to construct a molecular-MITT ( M-MITT) device (figure 1). We have found that the device's properties are better than of similar transistors in which the molecules are absent. The molecular transistor exhibits higher currents than the non-molecular device showing negligible leakage currents, with clear features which are attributed to the molecular properties.



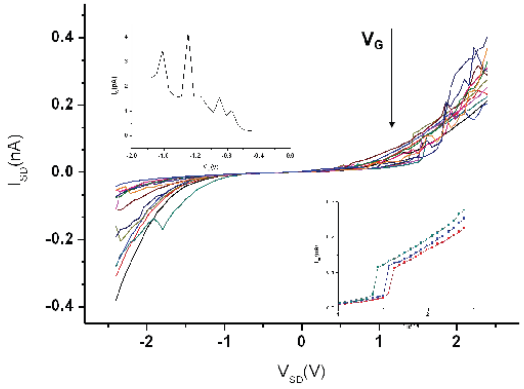




**Figure 1** ***Top left***. Schemes of the MITT (left) and of the M-MITT (right) structures and illustration of the CF. Materials used: (1) highly-doped silicon wafer, (2) 100nm-thick thermal oxide, (3) 80nm layer of $Si_3N_4$, Aluminum / $Al_2O_3$ electrodes (4,5), (6) Pd top electrode, side-gate titanium column (7), and its oxide (8). For the molecular transistor, an additional layer of $C_{60}$-based SAM was included (9, and chemical structure). For the full fabrication process see supplementary information. ***Top right.*** Transistor characteristics of the MITT taken for gate voltages ranging from -1.5 to 0 volts. Insets: Bottom – representative F-N plots taken at gate voltages of -0.5, -0.4, and -0.6 volts. Top: Leakage current characteristics. ***Bottom.*** Transistor characteristics and leakage current measurements (top inset) of the MITT taken at the same conditions used for the MITT one. The appearance of the "molecular

| | |
|---|---|
| | fingerprints" at some gate voltages is shown at the bottom inset. |

## 2.2 Gated-controlled rectification behaviour of a molecular-based transistor

We have constructed novel type of charging transistor utilizing Ferrocene-based SAM attached to gold nano-particle. Our experiments are, to our knowledge, the first to exhibit an unconventional gate effect described which allows controlling the rectification of the transistor via the gate voltage. We primarily attribute the strong gate-dependence to charging of the gold nano-particles in the contacts, which in turn modifies the spatial profile of the voltage across the junction. We have also developed a simple theoretical model that supports this interpretation. Our fabrication and control techniques may provide a new handle on investigating gated molecular junctions. Thus the increased sensibility of the I-V characteristics to VG may be attributed to the novel gate design, in which the molecules experience a much stronger coupling to the gate.

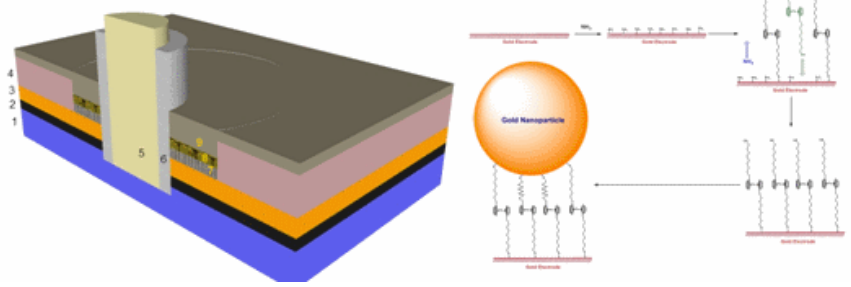



**Figure 2** *top* construction of the charging molecular transistor. The molecular layer includes a ferrocene SAM attached to Au

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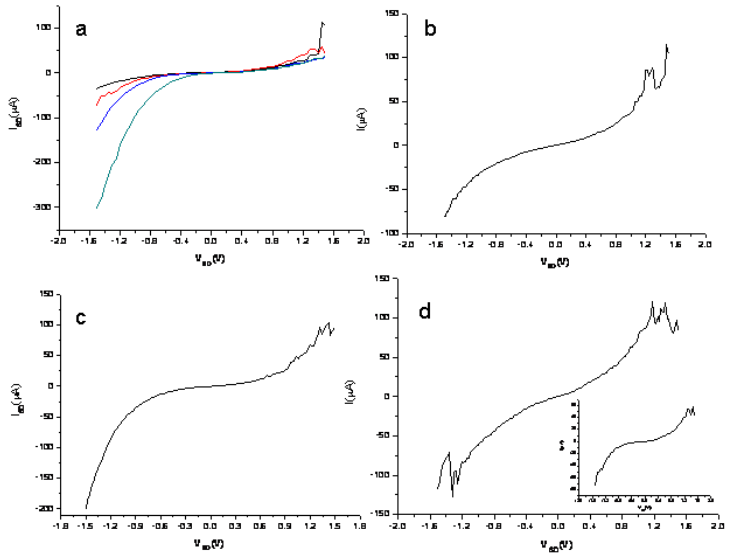
|  | nanoparticles *Bottom*. Current / voltage characteristics of the transistor demonstrating different modes of rectification. |

## 2.3 Construction and operation of three dimensional memory and logic molecular devices

**Note: Since this work is still unpublished- A more detailed description of the research is included.**

### 2.3.1 Background.

Organic and molecular electronics has emerged in the past few decades, and is drawing attention in part due to the potential for low-cost and large-scale production associated with this field. Moreover, scaling and performance improvement of traditional silicon-based microelectronic are expected to reach their physical limitations in the coming years, spurring the development of devices made from alternative material systems. Indeed, organic electronic devices such as field effect transistors, diodes, rectifiers and nanowires have been recently demonstrated. In this context, a useful electrical property that is inherent to several conducting and semiconductor polymers is negative-differential resistance (NDR), referring to a region in the current-voltage characteristics (I/V) of a device, in which an increase in applied voltage results in a decrease in measured current. "Traditional" NDR devices such as resonant tunnel diodes (RTD) or Gunn diodes, are commonly made of III-V semiconductors, and have been incorporated in high-frequency RLC oscillators and rectifier circuits. In the pre-CMOS era, RTDs have been used to construct digital circuits, operating on the principle of monostable-bistable transition

(MBT), inherent to NDR devices. However, the costly fabrication processes associated with these devices has lead to their infrequent usage.

In the last year we have demonstrated a low-cost, plastic-based NDR device, showing robust and highly-reproducible IV characteristics. From these devices, a simple digital circuit was constructed and operated.

### 2.3.2 Results

The basic structure of the NDR device is shown in Figure 3. The device consisted of a monolayer of either n-octanethiol (C8H18S), self-assembled over an Au bottom electrode (cathode). The monolayer was formed in a predefined nanocavity, and laterally encapsulated by a layer of Si3N4 insulator, similar to work done by Akkerman et al. A layer of the conductive polymer blend PEDOT:PSS polymer (60 nm thick, fig 3b) was then spin-coated over the sample, forming a soft contact to the monolayer. Lastly, an Ag top electrode, serving as an anode, was evaporated over the alkanethiol/PEDOT:PSS stack. The device was fabricated in large scale on a silicon wafer with a thermally grown SiO2 layer. Additional fabrication and characterization details are provided in the Supplementary section.

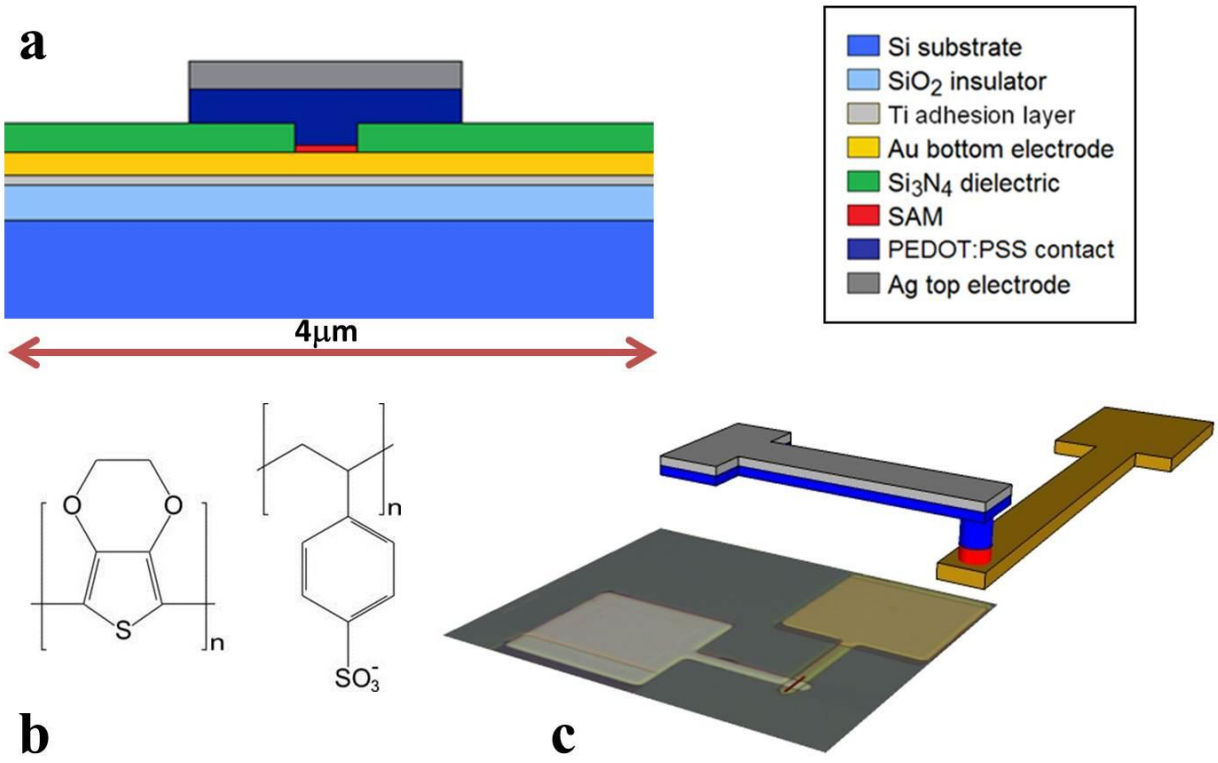



Figure 3. Structure of NDR device (dimensions not to scale). a. Cross-sectional schematic of a single device around the nanopore. b. Chemical structure of PEDOT:PSS. c. Three-dimensional schematics of the active area (top) and (bottom) an optical image of a single NDR device (red line represents the structure shown in Fig 3a.

I/V curve measurements of the devices were taken at room temperature, by conducting 0–3.5V voltage sweeps, using a Keithley 2636 source meter. A robust and repeatable NDR region was observed in the majority of devices measured, as shown in Figure 4. Specifically, 40 of the 50 devices that were measured (80%) display curves similar to those shown in Figure 4. For these devices, the NDR region was observed at a bias of 1.40 ± 0.11V, followed by valley currents of observed at a bias of 2.11 ± 0.10V. Peak-to-valley ratios for these devices ranged from 2.2–5.9. The remaining 10 devices also produced similar I/V curves showing an NDR region, however these were consistently noisier, and with lower peak and valley currents. These results are attributed to poorly formed or loosely-packed alkanethiol monolayers26. Similar I/V curves to these 10 devices were also observed in NDR devices that were not deposited with any monolayer.

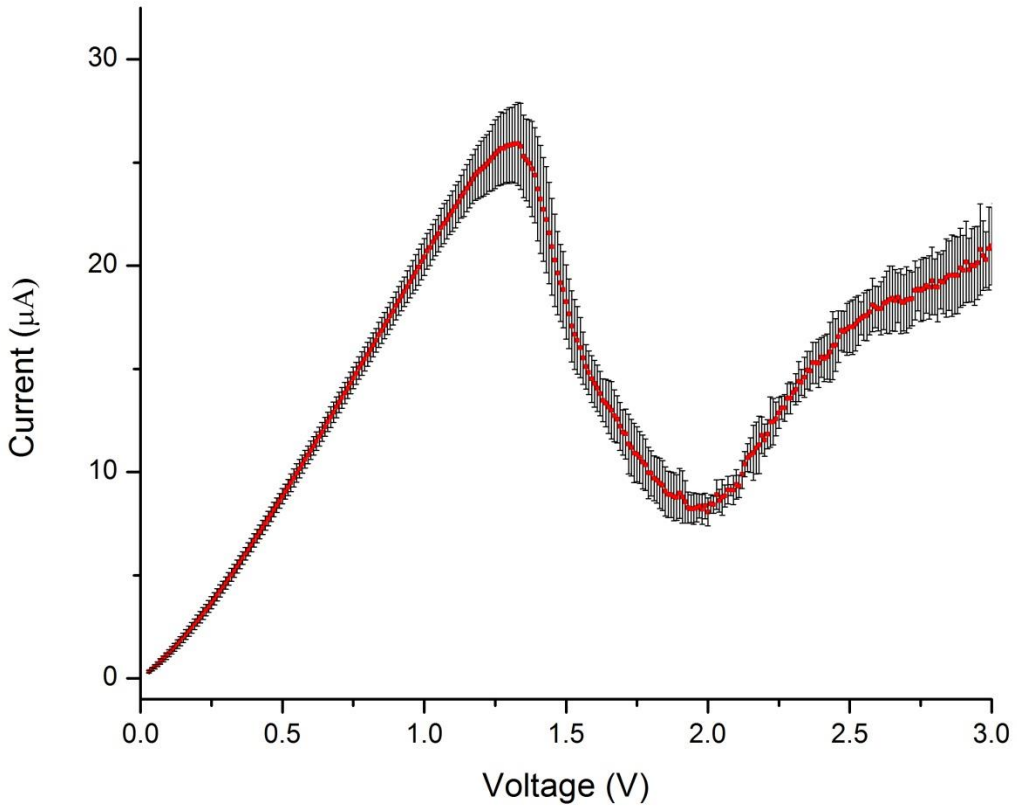



Figure 4. Measured IV curve of a representative NDR device. An average I/V curve (red dots) of five consecutive voltage sweeps and the relative error bars (black) taken for single NDR device.

We suggest the mechanism for NDR in all the devices is a result of accumulation of negative charge in trap states, forming a space charge region that hinders electron transfer. Specifically, as the bias is increased during a voltage sweep, an increasing number of electrons released from the Ag anode fall into trap states at the Ag/PEDOT:PSS interface and within the PEDOT:PSS layer. The effect of the accumulating trapped charge is observed at a bias of ~1.40V, at which point mobile electrons are repelled from conducting through the PEDOT:PSS layer. Increasing the bias past ~2.11V, trapped electrons are de-trapped due to the higher electric field, dissipating the negative charge, thereby causing an increase in measured current past the NDR

region. The difference between the high and the low current devices is attributed to a lower Schottky energy barrier for electron transfer, at the interface of properly formed alkanethiol SAM and Au, caused by an increase in the dipole moment relative to the surface, due to the Au-S bond.

Next, a circuit consisting of two NDR devices in series was consequentially designed, as shown in Figure 5.

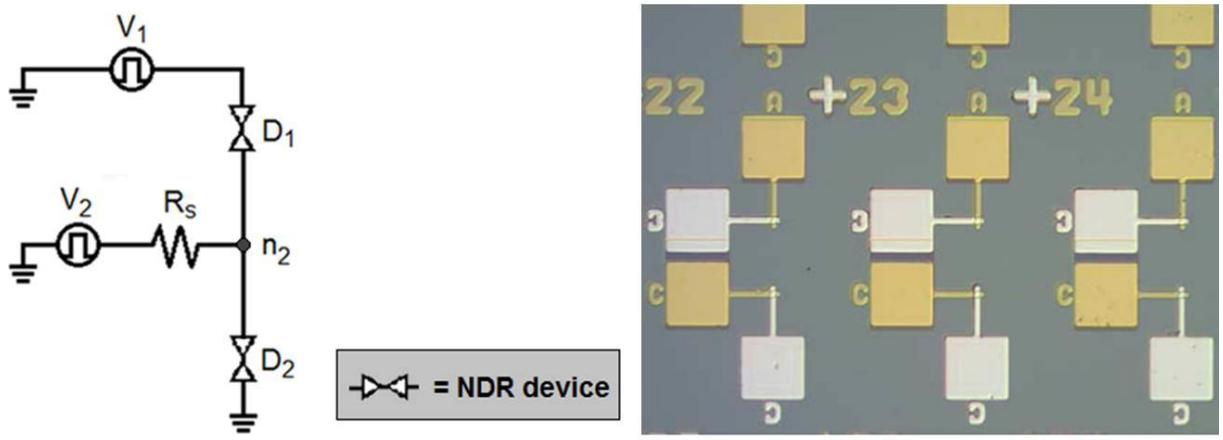



Figure 5 NDR-based logic gate circuit setup. Left – schematics. The circuit consisted of two NDR devices in series (D1, D2). Two voltage sources (V1, V2) were used as inputs. Resistor RS = 827kΩ. Output of the circuit was measured at node n2. Right. Optical image featuring an array of NDR devices used for circuit operation.

Simple nodal analysis at the junction n2 of NDR devices D1 and D2, and resistor RS shows that the voltage at the node is,

$$V(n_2) = \frac{R(D_2) \times R_S \times V_1 + R(D_1) \times R(D_2) \times V_2}{R(D_1) \times R(D_2) + R(D_1) \times R_S + R(D_2) \times R_S}$$

Due to the non-linear current response of D1 and D2, manifested in the resistances R(D1) and R(D2) of these devices, an analysis of the circuit as a logic gate was pursued, with the output measured at node n2 (figure 6a). It can be seen that the output characteristics includes several intersections points (see fig). We further show that pre-selected operation points in the vicinity of these intersections can be used to operate a logic gate circuit.

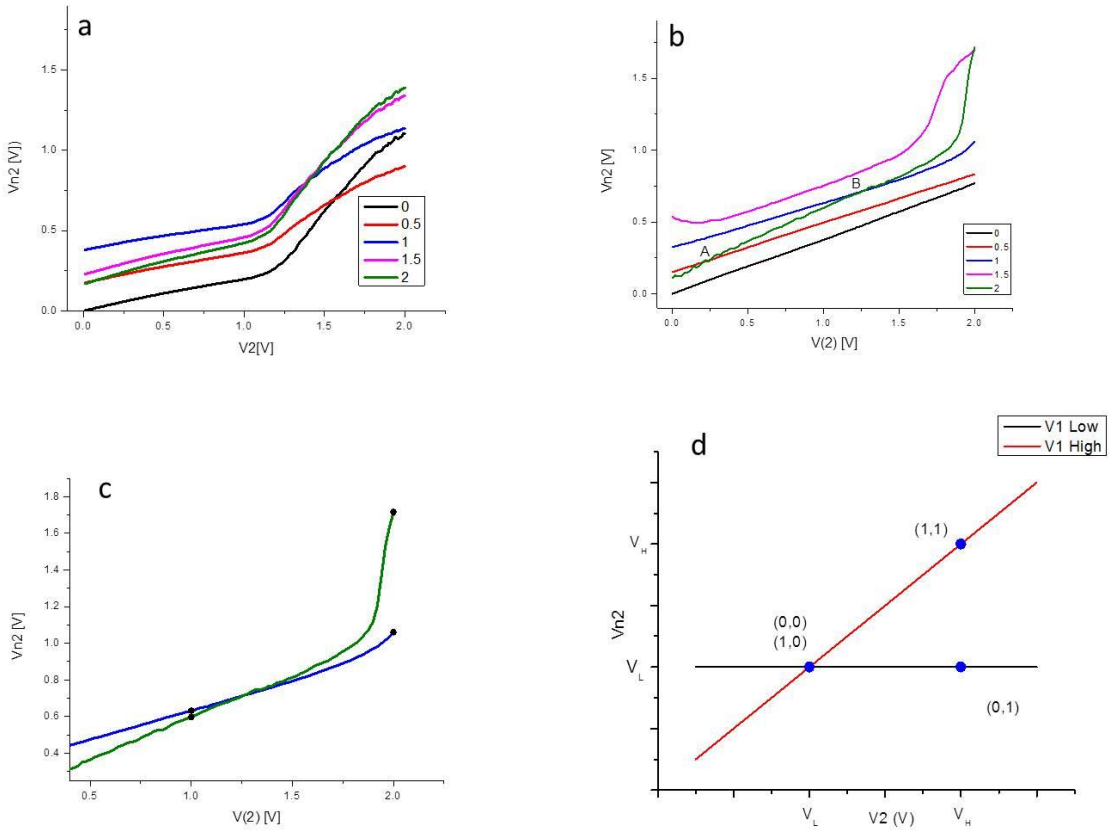



Figure 6 Simulated and measured "ideal" intersections. Simulated (a) and measured (b) family of curves plot. For the measured system V(n2) was measured five times consecutively. In each measurement V1 was set at a different bias, whereas V2 was swept from 0 – 2V (step=5mV). Intersection points are labeled as A and B. c, Highlight of intersection point B, along with the operation points and respective expected outputs, approximating AND functionality. d, V1 intersection for an "ideal" AND logic gate.

In order to observe any practical suitable operation points of the circuit, a methodology was devised in which the output voltage at node n2 was measured several times as a function of the inputs V1 and V2. For the first measurement, one input, V1 was held constant at 0V, while the other input, V2 was swept from 0–2V. In subsequent measurements, V1 was raised and held at increments of 0.5V, while V2 was again swept from 0–2V, for a total of 5 measurements. The resultant family-of-curves plot are shown in Figure 6b,c which shows reasonable similarity to the simulated data.

In Figure 6b,c, points A and B indicate intersections of two curves. Interpreting these intersections, it is possible to see that the same output voltage V(n2) is achieved for multiple values of input voltage V1. For example, intersection point B is highlighted in Figure 6c. Biasing V2 at 1.26V, V1 bias of either 1V or 2V will result in an output voltage of 0.72V for V(n2). This concept is readily applicable in the case of logic gates. Figure 6d depict the intersections and operation points of ideal AND gate. For an AND gate circuit, biasing V2 at VL, an input bias on V1 of either VL or VH will produce an output bias of V(n2)=VL. This is indicated by the intersection in Figure 6d. The same output of V(n2)=VL is achieved when V1=VL and V2=VH, as indicated by the bottom-right point in Figure 6c. Only when biasing V1 and V2 at VH, an output of V(n2)=VH is achieved, as indicated by the top-right point in Figure 6d. By setting VL and VH as digital values “0” and “1” respectively, AND functionality is apparent. Intersections and operation points of other ideal logic gate circuits are presented in the Supplementary section.

With the measured family-of-curves plot, the operation points of the logic gate circuit were chosen as VL=1V and VH=2V for both inputs V1 and V2. It is worth noting that the actual intersection at V2=1.26V was not chosen, in order for both inputs to maintain the same values. The expected output voltages for V(n2) are indicated for each of the four input combinations in Figure 6c, summarized in the table below.

It is apparent that for proper AND functionality, the values of VL and VH must be extended from 1V and 2V, to value ranges of ~0.6–1V, and ~1.7–2V, respectively.

To test the circuit at its derived operation points, two waveform generators (Agilent 33220A, Tabor WW5061) were used for inputs V1 and V2. These signals were generated as square waves with 50% duty cycle, with Vmin=1V, Vmax=2V, and frequencies of 1Hz and 2Hz, respectively, in order to cover all input combinations in one measurement. Both input voltages, along with the output voltage at node n2 were sampled using a LeCroy WaveAce 102 oscilloscope. Oscilloscope readout is presented in Figure 7. As can be seen, the output voltages largely reflect the expected values from Figure 7b and cover the complete AND truth table (table 1). However a noticeable spikes and voltage relaxation are observed. These observations, believed to occur due to charge/discharge mechanism of the NDR devices, place an upper limit on the frequencies at which the logic gate circuit can operate.

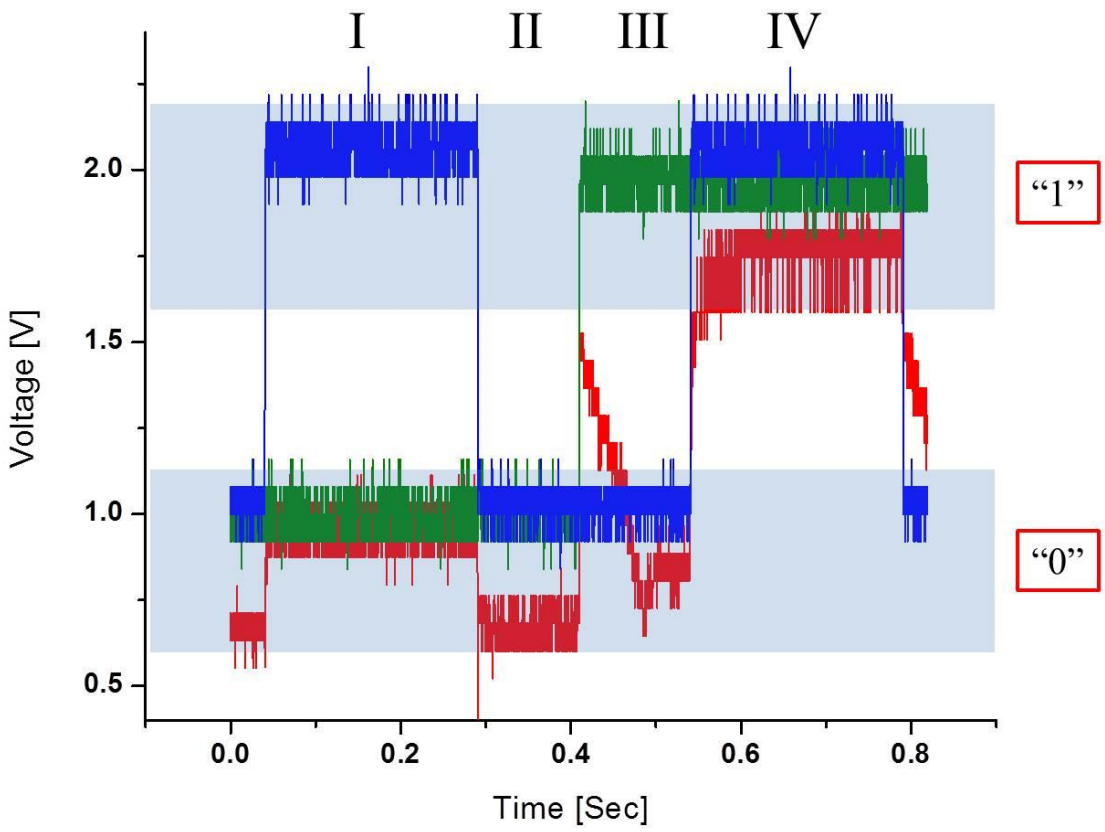



Figure 7 Input/output behavior of NDR-based AND logic gate circuit. V1 (Green ) and V2 (Blue) were defined as square waves (50% duty cycle, Vmin=1V, Vmax=2V, f = 1Hz, 2Hz, respectively). V(n2, Red)) was measured using a LeCroy WaveAce 102 oscilloscope over a 0.8092 sec. timeframe. Full logic operation of AND functionality presented as outputs of “0” and “1” is observed for all input combinations.

| Region (figure 7) | V1 | V2 | V(n2) |
|---|---|---|---|
| I | 1V (VL, “0”) | 2V (VH, “1”) | 1.061V (VL, “0”) |
| II | 1V (VL, “0”) | 1V (VL, “0”) | 0.632V (VL, “0”) |
| III | 2V (VH, “1”) | 1V (VL, “0”) | 0.597V (VL, “0”) |
| IV | 2V (VH, “1”) | 2V (VH, “1”) | 1.716V (VH, “1”) |

Table 1. Truth table of the NDR-based AND circuit

### 2.3.3 Discussion

We designed and fabricated a prototype of molecular circuit exhibiting a full "AND" logic operation. The circuit is compos of two NDR-based devices that are coupled in "GOTO" fashion. Numerous areas remain outstanding towards any possible adoption of the circuit for digital applications. Further optimization is required to find operation points that reduce the voltage ranges for VL and VH among I/O, in such a way that the intersections of V1 curves better approximate those of ideal logic gates. As the performance of the circuit currently stands, the spikes in output voltage that was observed during operation limits the circuit to the single-Hz range. Thus, further work is needed to determine the cause of these aberrations. Lastly, while the AND operation is commonly used in combinational logic circuits, it remains to be seen if operations that exhibit functional completeness, such as NAND and NOR could be implemented using the proposed NDR circuit and family-of-curves approach. Nonetheless, the organic NDR device presented in this work could be readily utilized in a variety of both analog and digital applications.

# 3 Related publications

## 3.1 Published


1. Gated-Controlled Rectification of a Self-Assembled Monolayer-Based Transistor, J. Phys. Chem. C, 117 (16), pp 8468–8474 (2013)
2. Towards Post-CMOS Molecular Logic Devices, R Hakim, ED Mentovich, S Richter; In Architecture and Design of Molecule Logic Gates and Atom Circuits, 13-24 (2013).
3. Doped Biomolecules in Miniaturized Electric Junctions, E Mentovich, B Belgorodsky, M Gozin, S Richter, H Cohen; Journal of the American Chemical Society 134 (20), 8468-8473, (2012)
4. Post-complementary metal-oxide-semiconductor vertical and molecular transistors: A platform for molecular electronics, ED Mentovich, S Richter; Applied Physics Letters 99 (3), 033108-033108-3 (2011)

5. Resolving the mystery of the elusive peak: negative differential resistance in redox proteins, ED Mentovich, B Belgorodsky, S Richter;The Journal of Physical Chemistry Letters 2 (10), 1125-1128 (2011)
6. High-Yield Fabrication of Molecular Vertical Junctions, ED Mentovich, N Rosenberg-Shraga, I Kalifa, A Tsukernik, N Hendler, M Gozin: Journal of Nanoscience and Nanotechnology 10 (12), 8260-8264 (2011)
7. 1-Nanometer-Sized Active-Channel Molecular Quantum-Dot Transistor, D Mentovich, B Belgorodsky, I Kalifa, S Richter: Advanced Materials 22 (19), 2182-2186 (2010)
8. Vertically Stacked Molecular Junctions: Toward a Three-Dimensional Multifunctional Molecular Circuit, ED Mentovich, I Kalifa, N Shraga, G Avrushchenko, M Gozin, S Richter; The Journal of Physical Chemistry Letters 1 (10), 1574-1579 (2010)
9. The role of leakage currents and the gate oxide width in molecular transistors, ED Mentovich, S Richter, Japanese Journal of Applied Physics 49 (1), 01AB04 (2010)
10. Construction and operation of sub-10 nm vertical molecular transistors, E Mentovich, S Richter:Nanoelectronics Conference (INEC), 2010 3rd International, 646-647 (2010)
11. Large-scale fabrication of 4-nm-channel vertical protein-based ambipolar transistors, ED Mentovich, B Belgorodsky, I Kalifa, H Cohen, S Richter:Nano letters 9 (4), 1296-1300 (2009)

## 3.2 Submitted

12. Logic-gate circuit composed of polymer-molecular junctions , Roy Hakim and Shachar Richter, Scintific reports (Nature open access) . Under revision (2013).